LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device comprising:

a substrate;

a plurality of inter-level dielectric (ILD) layers each formed of a dielectric material having a low dielectric constant (k);

at least one support structure disposed in each of the ILD layers at locations overlying each other so that support structures overly each other in the plurality of layers to mitigate structural damage of the ~~semiconductor device~~ plurality of ILD layers caused by stresses to the plurality of ILD layers;

at least one additional ILD layer having a dielectric constant which is higher than the ~~low-k~~ plurality of ILD layers, the at least one additional ILD layer overlying the ~~low-k inter-level dielectric~~ plurality of ILD layers; and

a contact layer overlying the at least one additional ILD layer and the support structures, wherein the at least one additional ILD layer isolates the contact layer from the support structures.

2. (Previously Presented) The semiconductor device of claim 1, wherein at least one ILD layer has an ultra low dielectric constant (k).

3. (Original) The semiconductor device of claim 1, wherein the at least one support structure is one of a trench and via formed from a support material.

4. (Original) The semiconductor device of claim 3, wherein the support material comprises at least one of aluminum, aluminum alloy, copper, copper alloy, tungsten, or tungsten alloy.

5. (Currently Amended) The semiconductor device of claim 1, wherein the support structure mitigates damage of the plurality of ILD ~~layer~~ layers due to forces applied onto the plurality of ILD ~~layer~~ layers during one of a subsequent processing and packaging of the semiconductor device.

6. (Cancelled)

7. (Previously Presented) The semiconductor device of claim 1, wherein the support structures are located underneath the source of the stress to mitigate damage to the semiconductor device.

8. (Original) The semiconductor device of claim 7, the source of the stress being a bond pad location.

9. (Cancelled)

10. (Currently Amended) The semiconductor device of claim 1, the support column ending at the at least one additional ILD layer.

11. (Cancelled)

12. (Currently Amended) A semiconductor device comprising:

a substrate;

a plurality of inter-level dielectric (ILD) layers each having a low dielectric constant (k);

~~at least one~~ a plurality of support ~~structure~~ structures disposed in each of the ILD layers at locations overlying each other so that support structures overly each other in the plurality of layers to mitigate structural damage of the ~~semiconductor device~~ plurality of ILD layers caused by stresses to the plurality of ILD layers;

at least one additional ILD layer having a dielectric constant which is higher than the ~~low-k~~ plurality of ILD layers, the at least one additional ILD layer overlying the ~~low-k inter-level dielectric~~ plurality of ILD layers;

a contact layer overlying the at least one additional ILD layer and the support structures, wherein the at least one additional ILD layer isolates the contact layer from the support structures;

wherein a plurality of support structures are disposed in the at least one of the ~~low-k~~ plurality of dielectric layers in an n x m matrix configuration, where n and m are integers greater than one; and

wherein the plurality of support structures are disposed at a location below a bond pad disposed on the semiconductor device.

13. (Currently Amended) The semiconductor device of claim 12, wherein [[a]] the plurality of support structures are disposed in the plurality of ILD layers ~~at least one low-k dielectric layer~~ at a plurality of locations spaced equidistant apart from each other across substantially the entirety of each of the plurality of ILD layers ~~entire layer~~.

14-23. (Cancelled)

24. (Currently Amended) A semiconductor device comprising:

a substrate;

a plurality of inter-level dielectric (ILD) layers each formed of a dielectric material having a low dielectric constant (k);

at least one support structure disposed in each of the ILD layers at locations overlying each other so that support structures overly each other in the plurality of layers to mitigate structural damage of the ~~semiconductor device~~ plurality of ILD layers caused by stresses to the plurality of ILD layers;

at least one additional ILD layer having a dielectric constant which is higher than the ~~low k~~ plurality of ILD layers, the at least one additional ILD layer overlying the ~~low k inter level dielectric~~ plurality of ILD layers; and

a bond pad overlying the at least one additional ILD layer and the support structures.

25. (New) The semiconductor device of claim 1, wherein the low dielectric constant (k) of the dielectric material of the plurality of ILD layers has a value between about 1.0 and about 3.8.

26. (New) The semiconductor device of claim 2, wherein the ultra low dielectric constant (k) of the dielectric material of the plurality of ILD layers has a value between about 1.0 and about 2.7.

27. (New) The semiconductor device of claim 1, wherein the at least one support structure is a plurality of support structures, the semiconductor device further comprising a solder bump overlying the contact surface, the plurality of support structures being located directly underneath the solder bump.

28. (New) The semiconductor device of claim 1, wherein the at least one support structure comprises a first plurality of support structures extending along a length of the semiconductor device and a second plurality of support structures extending along a width of the semiconductor device, the first and second plurality of support structures intersecting perpendicularly with respect to each other.

29. (New) The semiconductor device of claim 12, wherein the low dielectric constant (k) of the dielectric material of the plurality of ILD layers has a value between about 1.0 and about 3.8.

30. (New) The semiconductor device of claim 12, wherein the n x m plurality of support structures are configured such that the n support structures extend along a length of the semiconductor device and the m support structures extend along a width of the semiconductor

device, the plurality n support structures and the plurality m support structures intersecting perpendicularly with respect to each other.

31. (New) The semiconductor device of claim 24, wherein the low dielectric constant (k) of the dielectric material of the plurality of ILD layers has a value between about 1.0 and about 3.8.

32. (New) The semiconductor device of claim 24, wherein the at least one support structure is a plurality of support structures, the plurality of support structures being located directly underneath the bond pad.

33. (New) The semiconductor device of claim 24, wherein the at least one support structure comprises a first plurality of support structures extending along a length of the semiconductor device and a second plurality of support structures extending along a width of the semiconductor device, the first and second plurality of support structures intersecting perpendicularly with respect to each other.